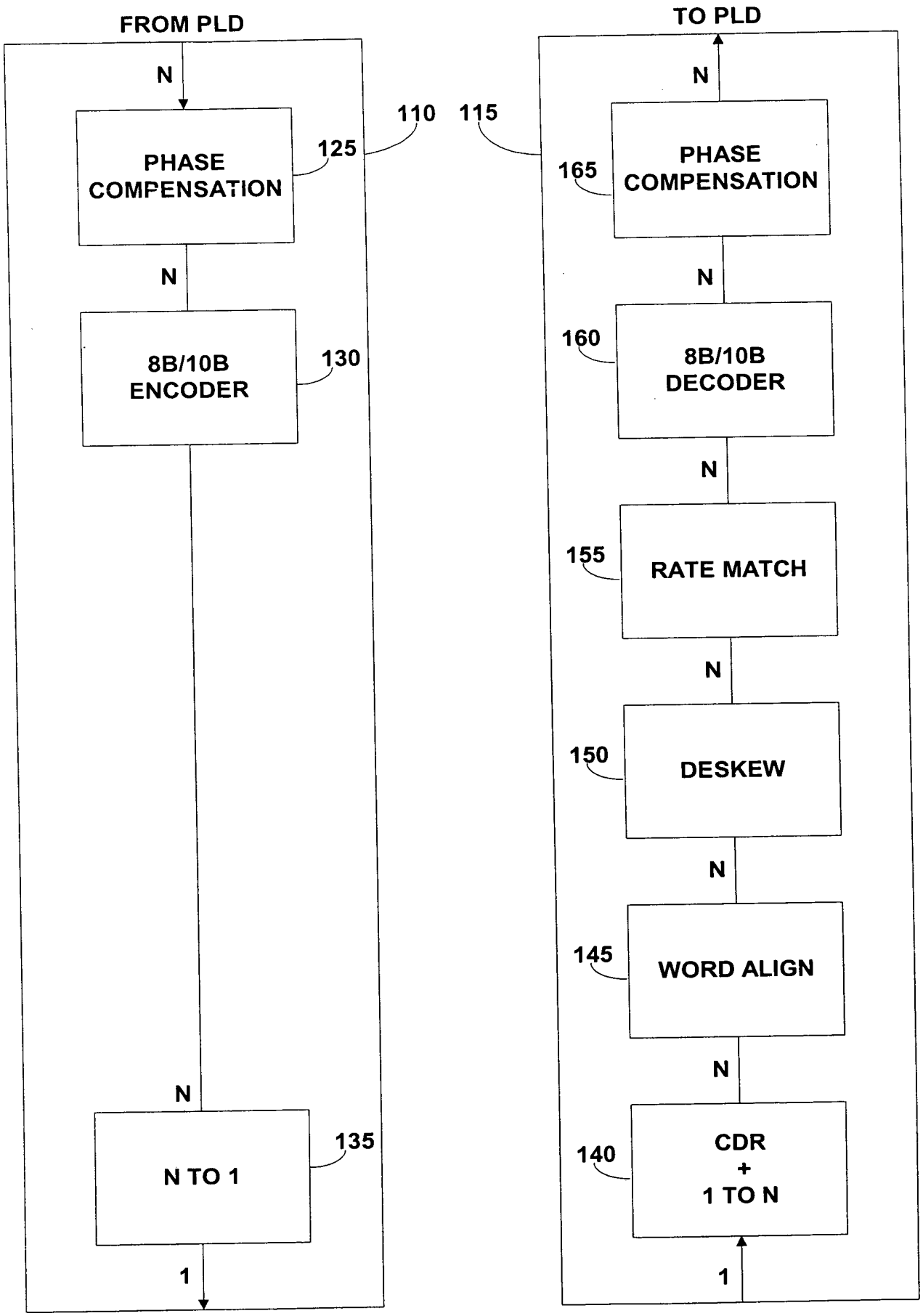
FROM PLD
N
PHASE COMPENSATION
125
110
N
8B/10B ENCODER
130
N
N TO 1
135
1
115
TO PLD
N
165
PHASE COMPENSATION
N
160
8B/10B DECODER
N
155
RATE MATCH
N
150
DESKEW
N
145
WORD ALIGN
N
140
CDR + 1 TO N
1

FIG. 1

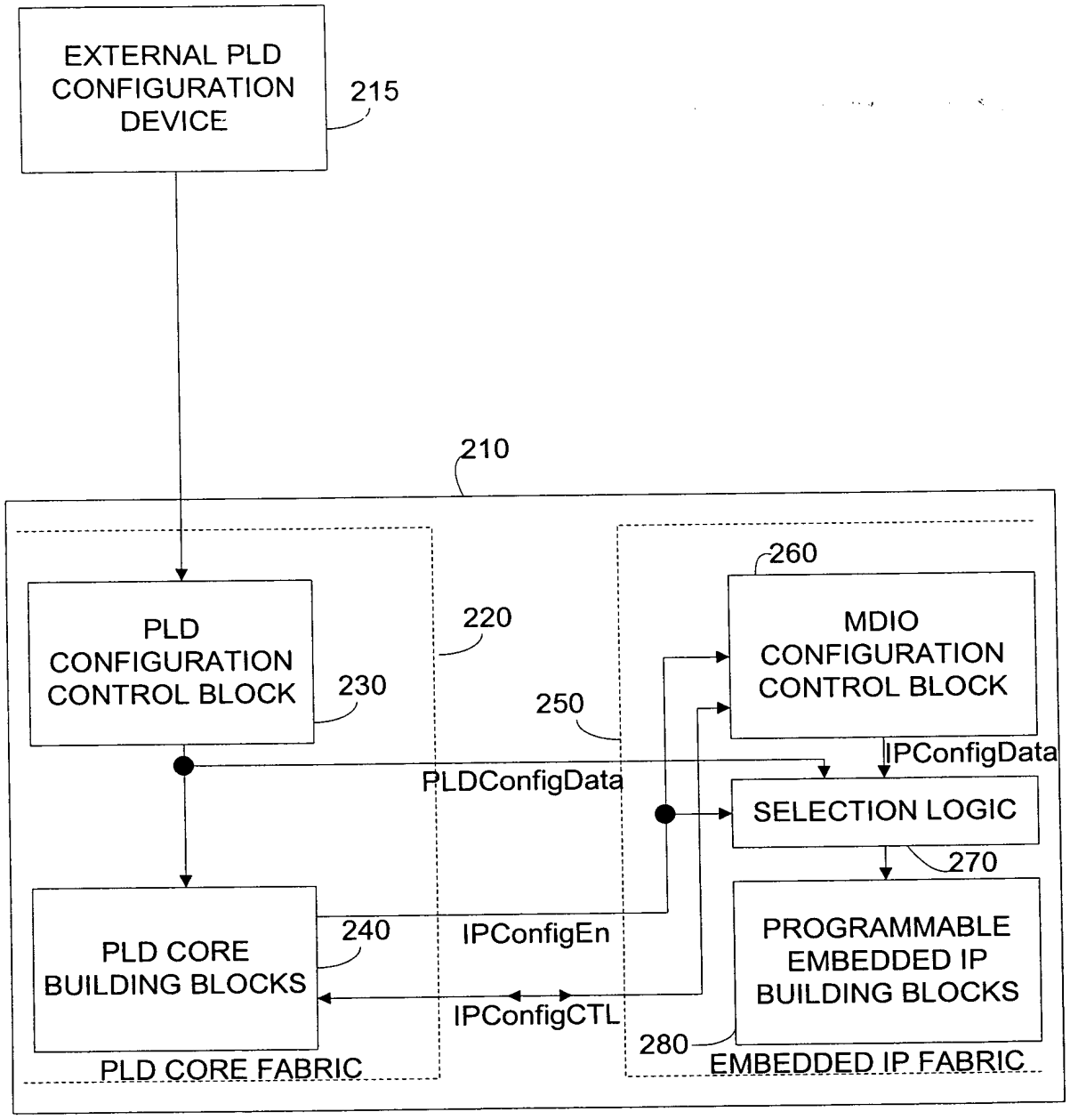
EXTERNAL PLD CONFIGURATION DEVICE
215
210
PLD CONFIGURATION CONTROL BLOCK
230
220
260
MDIO CONFIGURATION CONTROL BLOCK
250
IPConfigData
PLDConfigData
SELECTION LOGIC
270
PLD CORE BUILDING BLOCKS
240
IPConfigEn
IPConfigCTL
PROGRAMMABLE EMBEDDED IP BUILDING BLOCKS
280
PLD CORE FABRIC
EMBEDDED IP FABRIC

FIG. 2

	Management frame fields							
Frame	PRE	ST	OP	PRTAD	DEVAD	TA	ADDRESS / DATA	IDLE
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read inc.	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

FIG. 3